REMARKS

By the present amendment and response, independent claims 1 and 10 and dependent claims 2, 3, 5, 8, 12, 14, and 17 have been amended to overcome the Examiner's objections. Claims 1-18 are pending in the present application. Reconsideration and allowance of pending claims 1-18 in view of the following remarks are requested.

The Examiner has objected to the drawings. Applicant has amended Figure 1 to add a "(Prior Art)" legend. Applicant has enclosed herein 1 (one) replacement sheet including Figures 1, 2, and 3.

The Examiner has objected to the specification. Applicant has amended the specification as requested by the Examiner.

The Examiner has objected to the abstract. Applicant has amended the abstract as requested by the Examiner.

The Examiner has objected to claims 1, 3, and 10 due to informalities. Applicant has amended claims 1, 3, and 10 as suggested by the Examiner.

The Examiner has objected to claims 8 and 17 under 37 CFR 1.75(c). Applicant has amended claims 8 and 17 in response to the Examiner's objection and submits that the requirements of 37 CFR 1.75(c) have been met.

The Examiner has rejected claim 2 under 35 USC §112, second paragraph. Applicant has amended claim 2 in response to the Examiner's objection and submits that the requirements of 35 USC §112, second paragraph, have been met.

The Examiner has rejected claims 1-18 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,343,434 to Kenji Noguchi ("Noguchi") and further in view of U.S. patent number 5,646,948 to Kobayashi et al. ("Kobayashi"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 10, is patentably distinguishable over Noguchi and Kobayashi.

The present invention, as defined by amended independent claim 1, includes, among other things, a method for testing a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size. As disclosed in the present application, sectors in a memory device can be first sector type, such as a uniformly sized sector, or a second sector type, such as a boot sector. As disclosed in the present application, the present invention includes measuring at least one first time period related to erasing a first sector having a first sector type and establishing a first test limit based in part on the first time period. The present invention also includes measuring at least one second time period related to erasing a second sector having a second sector type and establishing a second test limit based at least in part on the second time period. As disclosed in the present application, the first and second test limits are used to determine whether the memory device passes or fails an erase test. As a result, the present invention advantageously achieves a method for testing a memory device, such as a flash memory device, that advantageously reduces the number of false rejects compared to a conventional approach using only a single test limit.

In contrast to the present invention as defined by amended independent claim 1, Noguchi does not teach, disclose, or suggest a method for testing a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size. Noguchi specifically discloses a method of testing a nonvolatile semiconductor memory device including determining whether an over-erased memory cell exists or not in a memory cell array in a bare chip state. See, for example, Noguchi, column 10, lines 56-60. However, Noguchi fails to teach, disclose, or suggest a method for testing a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size. Moreover, Noguchi fails to even mention different sector type memory sizes.

In contrast to the present invention as defined by amended independent claim 1, Kobayashi does not teach, disclose, or suggest a method for testing a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size. Kobayashi specifically discloses a method for testing "n" flash memories MUT_1, MUT_2, ... MUT_n that are in "n" test channels, respectively. See, for example, Kobayashi, column 4, lines 31-44. However, Kobayashi fails to teach, disclose, or suggest a method for testing a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size. In fact Kobayashi fails to even mention different sector type memory sizes. Thus, Kobayashi fails to cure the basic deficiencies in Noguchi.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not suggested, disclosed, or taught by Noguchi and Kobayashi, singly or in combination. As such, amended independent claim 1 is patentably distinguishable over Noguchi and Kobayashi. Thus, claims 2-9 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Noguchi and Kobayashi for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by amended independent claim 10, includes, among other things, a system for testing a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size. Amended independent claim 10 includes similar limitations as amended independent claim 1 discussed above. Thus, for similar reasons as discussed above, amended independent claim 10 is also patentably distinguishable over Noguchi and Kobayashi. Thus, claims 11-18 depending from amended independent claim 10 are, *a fortiori*, also patentably distinguishable over Noguchi and Kobayashi for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 10, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-18 pending in the present application are patentably distinguishable over the art cited by the Examiner. As

such, and for all the foregoing reasons, an early allowance of claims 1-18 pending in the present application is respectfully requested.

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